Architectures and Performance of AWG-based Optical Switching Nodes for IP Networks

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Abstract

In order to support the continuous growth of transmission capacity demand, optical packet switching technology is emerging as a strong candidate, promising to allow fast dynamic allocation of WDM channels, combined with a high degree of statistical resource sharing. This work addresses the design of optical switch architectures, based on previous proposals available in the technical literature that use an arrayed waveguide grating (AWG) device to route packets. Since the port number of currently available AWGs is a limiting factor, we propose two new modified structures which better exploit the switching capability of this component in the wavelength domain. Since a limited hardware complexity is a key requirement for all-optical switches, due to the high cost of optical components, these different node configurations are compared in terms of complexity. Traffic performance of these new structures in a full optical packet switching scenario is also examined.

Index Terms

Optical Packet Switching, All-Optical Networks, Arrayed Waveguide Grating, IP Network.

I. INTRODUCTION

IN the latest years telecommunication networks have been demanding an unprecedented, dramatic increase of capacity, fostered mostly by the exponential growth of Internet users and by the introduction of new broadband services. The IP architecture is being seen as the unifying paradigm for a variety of services and for making real the Broadband Integrated Services Digital Network (B-ISDN).

In order to face this challenge, considerable research is currently devoted to the design of IP fully-optical backbone networks, which will provide the possibility of overcoming the capacity bottleneck of classical electronic-switched networks.

A single optical fiber offers a potentially huge transmission capacity: just in the third wavelength window, tens of Terahertz are there to be mined, if only we could be able to exploit such tremendous bandwidth with adequate technology. In the last ten years, optical Dense Wavelength Division Multiplexing (DWDM) has been developed, bringing commercial systems which provide impressive transmission capacities: one Terabit per second per fiber, over distances on the order of 100 km, are feasible today with off-the-shelf components.

Moreover, recently DWDM has evolved to support some network functions as circuit routing and wavelength conversion and assignment. In WDM-routed networks, a wavelength is assigned to each connection in such a way that all traffic is handled in the optical domain, without any electrical processing on transmission.

Unfortunately, optical devices used in market equipment are not mature enough to meet packet-by-packet operation requirements yet. An interesting solution which tries to represent a balance between circuit switching low hardware complexity and packet switching efficient bandwidth utilization is the optical burst switching ([1], [2] and [3]). In an optical burst switching system, the basic units of data transmitted are bursts, made up of multiple packets, which are sent after control packets, carrying routing information, whose task is to reserve electronically the necessary resources on the intermediate nodes of the transport network.

Such operation results in a lower average processing and synchronization overhead than optical packet

switching, since packet-by-packet operation is not required. However packet switching has a higher degree of statistical resource sharing, which leads to a more efficient bandwidth utilization in a bursty, IP-like, traffic environment.

We address here the long-term view of a full packet switching network performing IP packet transport, in which optical operations are performed as much as possible exploiting the currently available optical device technology. Apparently most of the operations related to the packet header processing needs to be done in the electronic domain. This paper deals with the architecture of an optical packet switching node first proposed in [4][5], which is equipped with a fiber delay line stage used as an input buffer for optical packets. Two new alternative structures of the switching core of the node, which exploit the routing in the wavelength domain inherently available in the switching components being used, are described.

The paper is organized as follows. Sections II and III describe the optical network architecture we envision and the proposed architecture of an optical packet switching node. Section IV provides a comparison of the different solutions in terms of node complexity and traffic performance.

II. NETWORK ARCHITECTURE

The architecture of the optical transport network we propose consists of $M = 2^m$ *optical packet-switching nodes*, each denoted by an optical address made of $m = \log_2 M$ bits, which are linked together in a mesh-like topology. A number of *edge systems* (ES) interfaces the optical transport network with IP legacy (electronic) networks (see Fig. 1).

The transport network operation is *asynchronous*; that is, packets can be received by nodes at any instant, with no time alignment. The internal operation of the optical nodes, on the other hand, is *synchronous* or *slotted*, since the behavior of packets in an unslotted node is less regulated and more unpredictable, resulting in a larger contention probability.

An ES receives packets from different electronic networks and performs *optical packets* generation. The optical packet is composed of a simple optical header, which comprises the m-bit destination address, and of an optical payload made of a single IP packet or, alternatively, of an aggregate of IP packets. The

optical packets are then buffered and routed through the optical transport network to reach their destination ES, which delivers the traffic it receives to its destination electronic networks. At each intermediate node in the transport network, packet headers are received and electronically processed, in order to provide routing information to the control electronics, which will properly configure the node resources to switch packet payloads directly in the optical domain.

Header and payload of a packet are transmitted serially, as shown in Fig. 2, where header duration is equal to T_H and payload duration to T_P. At each switching node the optical header is read, dropped and regenerated at the node output; therefore, guard times (T_G) are needed in order to avoid payload/header superposition, due to clock jitter in the transmission phase. Hence, the total overhead time is equal to $T_{OH} = T_H + 2T_G$. Both header and payload are assumed to be transmitted at 10 Gb/s rate, which is compatible with current transmission technology.

Two critical parameters must be considered when dimensioning T_H and T_G: the maximum header processing time (T_{proc}) and the switching time of the slowest switching element (T_{sw}) in the node (see Sec. III). During header processing time, the node decodes the optical header and processes the carried information, performing packet routing and contentions resolution (as explained later). In order to compensate this processing time, a delay line should be inserted at each node input, delaying all incoming payloads by a T_{proc} interval, so that payloads enter the node when all header processing has been performed. Finally, considering that the optical header is dropped at the node input, the silence between two consecutive payloads is equal to T_{OH} and so it will be necessary that $T_{OH} > T_{sw}$.

Given these considerations, an overhead time $T_{OH} = 8$ ns has been chosen, with header duration $T_H = 6$ ns and guard times $T_G = 1$ ns. Thus an 8 ns interval is available to perform switching, and a 10 bit jitter at 10 Gb/s is tolerated in header regeneration. Moreover, this value of T_H implies a 60 bit header. In [6] a 10 Gb/s optical packet receiver is demonstrated, using a 40 bit-long preamble. Therefore, the remaining 20 bits will carry packet information: 5 bits are reserved for packet length (expressed in time-slots, for a maximum value of $2^5 - 1 = 31$ time-slots), and the remaining 15 bits for the destination

ES address (up to a maximum of 2^{15} edge-systems). Supporting more information in the packet header, such as time stamping, optical priority labels, etc, is outside the scope of this paper.

We chose a slot duration (T) equal to the time duration of an optical packet whose payload consists of the smallest TCP/IP packet (i.e. 320 bits, the size of an IP packet carrying a TCP acknowledgment). Time-slot duration is therefore equal to $T = T_{OH} + 32$ ns $= 40$ ns. Owing to our assumption of slotted operation, it takes a number $\left\lceil \frac{T_{OH} + T_P}{T} \right\rceil$ of slots to switch (and transmit) an optical packet with overhead time T_{OH} and payload time T_P. Fig. 3 shows the case of an IP packet engaging two slots. Note that, under these assumptions, a 1500-byte packet (i.e. the maximum Ethernet payload length) will fill in a 31 time-slot long optical packet. Since a small traffic fraction is composed of longer packets in current IP networks (see [7]), most of the electronic information units will not need to be segmented in order to travel through the optical network. A more accurate choice of the time-slot duration is left for further study, when detailed and accurate traffic models will be considered.

III. Node Architecture

The general architecture of a network node is shown in Fig. 4. It consists of three stages: a first stage of channel demultiplexing, a second stage of switching and a third stage of channel multiplexing. The node is fed by N incoming fibers each having W wavelengths. In the first stage the incoming fiber signals are demultiplexed and G wavelengths from each input fiber are fed into each one of the W/G second-stage switching planes, which constitute the switching fabric core. Once signals have been switched in one of the parallel planes, packets can reach every output port through multiplexing carried out in the third stage using any of the G wavelengths that are directed to each output fiber. We note that the number of inlets of each third-stage multiplexer varies, depending on the specific structure of the switching planes. Wavelength conversion must be used for contention resolution, since at most G packets can be concurrently transmitted by each second-stage plane on the same output link.

The detailed structure of one of the W/G parallel switching planes is presented in Fig. 5. It consists of three main blocks: an input *synchronization unit*, as the node is slotted and incoming packets need to

be slot-aligned, a *fiber delay lines unit*, used to store packets for contention resolution, and a *switching matrix unit*, adopted to achieve the switching of signals.

These three blocks are all managed by an *electronic control unit* which carries out the following tasks:

- optical packet header recovery and processing;

- managing the synchronization unit in order to properly set the correct path through the synchronizer for each incoming packet;

- managing the tunable wavelength converters inside the delay unit and in the switching matrix, in order to properly delay and route incoming packets.

One electronic control unit is implemented in each switching plane and, since at each plane output packets are transmitted using one of the G input wavelengths, the controllers' job is carried out in a completely parallel and independent way.

A. Synchronization Unit

This unit consists of a series of 2×2 optical switches interconnected by fiber delay lines of different lengths. These are arranged in a way that, depending on the particular path set through the switches, the packet can be delayed for a variable amount of time, ranging between $\Delta t_{min} = 0$ and $\Delta t_{max} = 2(1 - (1/2)^{n+1}) \times T$, with a resolution of $T/2^n$, where T is the time slot duration and n the number of delay line stages.

The synchronization is achieved as follows: once the packet header has been recognized and packet delineation has been carried out, the packet start time is identified and the control electronics can calculate the necessary delay and configure the correct path of the packet through the synchronizer.

Due to the fast reconfiguration speed needed, fast 2×2 switching devices, such as 2×2 semiconductor optical amplifier (SOA) switches [8] that have a switching time in the nanosecond range, must be used.

B. Fiber Delay Lines Unit

After packet alignment has been carried out, the routing information carried by the packet header allows the control electronics to properly configure a set of tunable wavelength converters (TWC), in order to deliver each packet to the correct delay line to resolve contentions. An optical packet can be stored for a time slot, with a 40 ns duration, in about 8 meters of fiber at 10 Gbps. To achieve wavelength conversion several devices are available [9], [10], [11].

The delay lines are used as an *optical scheduler*. This policy uses the delay lines in order to schedule the transmission of the maximum number of packets onto the correct output link. This implies that an optical packet P_1, entering the node at time αT from the i-th WDM input channel, can be transmitted after an optical packet P_2, entering the node on the same input channel at time βT, being $\beta > \alpha$. For example, suppose that packet P_1, of duration $l_1 T$, must be delayed for d_1 time slots, in order to be transmitted onto the correct output port. This packet will then leave the optical scheduler at time $(\alpha + d_1)T$. So, if packet P_2, of duration $l_2 T$, has to be delayed for d_2 slots, it can be transmitted before P_1 if $\beta + d_2 + l_2 < \alpha + d_1$ since no collision will occur at the scheduler output. Previous works considered the employment of *optical FIFO buffering*, but optical scheduling obviously resulted a better choice. The reader is referred to [4] for a deeper analysis of this topic.

Given the maximum achievable delay D_{max} slot, for each switch input $D_{max}+1$ delay lines are needed, with delays growing from 0 to D_{max}. Moreover, NW multiplexers and demultiplexers with $D_{max} + 1$ input and output ports are needed to perform packet buffering.

C. Switching Matrix

Once packets have crossed the fiber delay lines unit, they enter the switching matrix stage in order to be routed to the desired output port. This is achieved using a set of tunable wavelength converters combined with an arrayed waveguide grating (AWG) wavelength router [12].

The AWG is used as it gives better performance than a normal space switch interconnection network,

as far as insertion losses are concerned. This is due to the high insertion losses of all the high-speed all-optical switching fabrics available at the moment, that could be used to build a space switch interconnection network. Commercially available 40 channel devices have a channel spacing of 100 Ghz and show an insertion loss of less than 7.5 dB [13].

Three different structures are proposed for the realization of this stage, referred to as structure (a), (b) and (c). In the following sections we will consider single plane structures, that is $W = G$, in which the switching matrix has NW inlets and NW outlets. The extension to multi-plane nodes is easily achieved for the first two structures by selecting $W' = W/G$. The third structure will require further considerations.

1) Structure (a): The simplest switching matrix structure, first proposed in [4], is shown in figure 6. It consists of $2NW$ tunable wavelength converters and an AWG with size $NW \times NW$. Only one packet is routed to each AWG outlet and this packet must finally be converted to one of the wavelengths used in the WDM channel, paying attention to avoid contention with other packets of the same channel. This solution is therefore *Strict Sense Non-Blocking*.

2) Structure (b): In order to reduce the number of planes of the node and thus to better exploit the *channel* grouping effect (i.e. the sharing of different channels for transmitting a large number of packets, the load per channel being constant) more than one packet can be routed in each AWG inlet; apparently the packets sharing the same input must be transmitted on different wavelengths. The structure of the AWG, in fact, is such that different wavelengths entering the same input port will emerge on different output ports, as shown in figure 7 in the case of four incoming and outgoing fiber channels, each supporting four wavelengths.

In the switching matrix structure illustrated in figure 8, up to k different packets are sent to the same AWG inlet using different wavelengths. A simple node design requires k to be an integer that divides W. From AWG input port i, the output channel j can be reached by W/k different packets, since there are exactly W/k AWG outlets connected to that channel. During each time slot, up to W packets can be routed to the same AWG outlet using different wavelengths. Hence, demultiplexers are needed to

split the different signals and to route them to the last stage of wavelength converters. If $k \leq W/k$, no contention can happen in the multiplexing stage, so this structure behaves exactly as a structure (a) with size $NW \times NW$. On the other hand, when $k > W/k$, events of packet blocking occur, considering the fact that W/k paths are available to reach a tagged output for up to k packets per inlet. So, when more than W/k packet in the same AWG inlet are destined to the same output channel, a contention happens, even if the total number of packets addressed to that output is smaller than W.

3) Structure (c): Node structure (b) can be simplified by selecting $k = N$, so that each AWG input can receive up to N packets using different wavelengths. Therefore, the number of AWG inlets is now exactly W. In this last structure the last TWC stage isn't needed anymore, provided the employed AWG works on the same wavelengths used in the outgoing fibers. In fact, if the electronic controller takes care of avoiding wavelength contention between AWG outlets connected to the same output channel, packets are ready to be transmitted as soon as they exit the AWG. Therefore, a packet entering the AWG inlet i and destined to the output WDM channel j can not be transmitted using every color in the WDM channel, but only using a subset which consist of the W/N wavelengths through which the packet can reach the desired output channel, thus reducing the benefits of *channel grouping* (when N and W are kept constant).

We would like to point out that the size $W \times W$ of the AWG is not a limiting factor for this node architecture, since the current optical technology enables using optical fibers supporting a number of wavelengths much larger than the maximum size of an AWG. On the other hand if we are willing to fully exploit the external number of wavelengths W in the internal node structure in case of a maximum size $W' \times W'$ of the AWG, with $W' \leq W$, a multi-plane structure must be adopted.

In order to arrange a multi-plane structure, the key point is the wavelength splitting among planes, so that the minimum spacing between adjacent wavelengths in a plane is compliant with the AWG requirements. Let us suppose to use W wavelengths per channel with Δf spacing and to adopt $W/j \times W/j$ AWGs with channel spacing $j\Delta f$, where j is an integer. Then, the WDM channels should be split into j wavelengths combs with $j\Delta f$ spacing, whereas in the overall comb wavelengths are spaced by Δf. Fig. 10 represents

this situation for $j = 2$. Furthermore, the used AWGs should be built in order to have Δf-spaced central wavelengths.

IV. COMPLEXITY AND PERFORMANCE COMPARISON

In order to evaluate the three different switching structures, we will first examine the packet loss probability of a simplified network scenario, where an analytical model can easily be obtained. We will later compare the complexity of the structures in terms of number of components, and finally their traffic performance under a more realistic traffic assumption and a more complex configuration will be analyzed.

A. Switching Capability

In order to perform a basic comparison among the switching capabilities of the the different structures, the following assumptions are made:

- no input buffering is performed;
- packet length is constant, equal to the time-slot duration.

In this simple case, a packet is offered by each single wavelength channel with probability p in each time slot, where p is the offered load per wavelength. We can easily derive an analytical model of the structure (a) and (b) of switching matrices.

1) Structure (a): Let us define:

$$\beta\left(n, i, p\right) = \binom{n}{i} p^i \left(1 - p\right)^{n-i}.$$

The probability that exactly i packets are addressed to a tagged output channel is then

$$a\left(i\right) = \beta\left(NW, i, \frac{p}{N}\right).$$

If X denotes the number of packets addressed to the tagged output, the carried load per wavelength can be expressed as

$$
\begin{aligned}
\rho_C &= \frac{1}{W}\left[\sum_{i=1}^{W-1} i \cdot \mathrm{Pr}\left(X = i\right) + W \cdot \mathrm{Pr}\left(X \geq W\right)\right] = \\
&= \frac{1}{W}\left[\sum_{i=1}^{W-1} i a\left(i\right) + W\left(1 - \sum_{i=0}^{W-1} a\left(i\right)\right)\right].
\end{aligned}
\tag{1}
$$

Since p represents the offered load per wavelength ρ_O, the loss probability is given by

$$P_L = 1 - \frac{\rho_C}{\rho_O} = 1 - \frac{\rho_C}{p}. \tag{2}$$

2) Structure (b): Let us define $c(m,i)$ as the probability that i packets in m AWG inlets are addressed to the tagged output port, with W/k or less packets per inlet:

$$c(m,i) = \begin{cases} \beta\left(mk, i, \frac{p}{N}\right) & 0 \leq i \leq \frac{W}{k} \\ \sum_{j=0}^{\frac{W}{k}} c(m-1, i-j)\,\beta\left(k, j, \frac{p}{N}\right) & \frac{W}{k} < i \leq m\frac{W}{k} \\ 0 & i > m\frac{W}{k} \end{cases}$$

Once defined the probability that more than W/k packet are addressed to the tagged output in a single AWG inlet as

$$p_b = 1 - \sum_{i=0}^{\frac{W}{k}} \beta\left(k, i, \frac{p}{N}\right),$$

the probability that the number of packets that can be routed to the desired output is exactly i , after contention resolution in the multiplex stage, is expressed as

$$b(i) = \sum_{j=0}^{\left\lfloor \frac{i}{W/k} \right\rfloor} \binom{\frac{NW}{k}}{j} p_b^j\, c\left(\frac{NW}{k} - j, i - \frac{jW}{k}\right).$$

Therefore, as seen for the original structure in (1)

$$\rho_C = \frac{1}{W}\left[\sum_{i=1}^{W-1} i\,b(i) + W\left(1 - \sum_{i=0}^{W-1} b(i)\right) \right],$$

and the loss probability is given again by (2).

Packet loss probability of the proposed structures are now compared using the previous analytical models for structures (a) and (b), whereas computer simulation has been used for structure (c). Figures 11 and 12 show the loss probability of the different switching matrices, when employing a single-plane structure to switch 2 and 4 WDM channels, with 12 different wavelengths. This value of W has been chosen because it enables us to compare the three structures with different parameters. No results were plotted for $k = 3$ and $k = 2$, since in these cases $k \leq W/k$, and so the loss probability is the same as

that of the structure (a). As it could easily be foreseen, the original structure outperforms the other two, but it uses AWG with larger size.

The results in figure 13, where the different structures are compared with 8×8 AWGs, are far more interesting. Again, only values of k such that $k > W/k$ have been considered. It can be seen that structure (c) behaves a little better than structure (a), whereas structure (b) leads to better performance for small values of k. As k is increased, the loss probability grows and reaches that of structure (a) when $k = 8$. Larger values of k lead to worse performance. It is interesting to note that structure (b) performs exactly the same as structure (a) when $k = 8$. In the appendix it is shown that whenever $k = \sqrt{NW}$, the performance of structure (b) is equal to that of structure (a) with $W' = W/k$.

B. Complexity

In table I the components needed to build a switching matrix with size $NW \times NW$ are listed. Structure (b) doesn't seem to be cost-effective, since if $NW/k^2 > 1$ the number of TWCs will grow quickly. Structure (c) greatly reduces the costs but, as seen in section IV-A, it is not competitive with the original structure when packet loss performance is evaluated. On the other hand, table II reports a cost comparison of the different structures keeping constant the AWG size[1]. In this case, structure (c) doesn't only behave better than original (as was previously seen), but also reduces implementation costs.

C. Performance Results

We show now some traffic performance results given by the different node architecture configurations obtained through computer simulation. Packet interarrival has been modeled as a Poisson process with negative exponential interarrival times. Based on measurement of real IP traffic [7], the following packet

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[1]Note that under this hypothesis structure (a) needs to be implemented in a multi-plane node.

length distribution has been assumed:

$$
\begin{cases}
p_0 = P(L = 40 \text{ bytes}) = 0.6 \\[2mm]
p_1 = P(L = 576 \text{ bytes}) = 0.25 \\[2mm]
p_2 = P(L = 1500 \text{ bytes}) = 0.15
\end{cases}
$$

In this traffic model, the resulting average packet length is 393 bytes. Only structures (a) and (c) have been examined now, considering the fact that the implementation of structure (b) brings to an increase of complexity of the electronic controller. On the other hand, in order to implement structure (c), it is only necessary to add a $W \times N$ table to the electronic controller, where each entry contains the W/N wavelengths that can be used to route a packet from inlet i to output channel j. Moreover, this structure reduces the complexity of the controller operations in each time slot, because W/N output wavelengths per packet must be considered, rather than W.

Given the results of section IV-A, the two switching matrices are compared keeping constant the AWG size. Figures 14 and 15 show a performance comparison for several values of the maximum buffer depth D_{max}. Structure (c) outperforms the original structure (a) and the improvement is as greater as the maximum buffer depth is increased. This improvement is also much bigger as traffic load is decreased.

The number of wavelengths per channel connected to every switching plane is a key parameter to improve node performance, due to the *channel grouping* phenomenon, as was pointed out in [4] and [5]. In figure 16, different configurations with 32×32 AWGs are compared. It is shown that structure (c), where the value of the G parameter is equal to 32, always gives better results.

V. CONCLUSIONS

In this work we have proposed and compared different architectures of the switching core for an IP over WDM switching fabric. Starting from previous proposals of AWG-based optical switching node, it has been shown how to arrange the switch core so as to perform the switching also in the wavelength domain, by thus fully exploiting the AWG properties. Two different architectural solutions have been examined and compared in terms of complexity and traffic performance. The results are quite promising

in that under reasonable assumptions on the offered IP traffic, the simplest of the new proposed structures outperforms the original one. Other issues will have to be addressed in the future such as the behavior of this new structure when recirculation delay lines are added to obtain *shared buffering*, especially compared to the results given in [5] for the original structure. Finally, it would be useful to compare the obtained performance results with those given by available electronic routers; regrettably, due to immaturity of current optical switching technology, a comparison between these the two scenarios is not feasible yet. Consider, for example, that it is possible to equip electronic routers with Gigabytes of Random Access Memory at relatively low costs, while eight meters of fiber are needed to provide the capacity necessary to store just a single one-slot optical packet in the optical domain.

APPENDIX

Let us consider a switching matrix with structure (b) called S_b with parameters N_b, W_b, $k = \sqrt{N_b W_b}$, with packet loss probability π_b, and a structure (a) called S_a with parameters $N_a = N_b$ and $W_a = W_b/k = \sqrt{W_b/N_b}$, with packet loss probability π_a. It can be easily shown that

$$\pi_a = \pi_b.$$

In structure S_b, after the multiplexing stage, up to W_b/k packets per inlet are feasible to enter the AWG addressed to a tagged output. Being $N_b W_b/k$ the number of AWG inlets, the total number of packets which will request the tagged output channel will be upper bounded by

$$\frac{N_b W_b^2}{k^2} = \frac{N_b W_b^2}{N_b W_b} = W_b.$$

Therefore no contention happens in the AWG stage. Let us now examine the multiplexing stage. At each multiplexer, up to k packets can contend for the tagged output, and only W_b/k packets will win contention. This is the same situation that happens in the structure S_a, where up to $N_a W_a$ packets contend for the output and only W_a win, and

$$N_a W_a = N_b \sqrt{\frac{W_b}{N_b}} = \sqrt{N_b W_b} = k$$

$$W_a = \frac{W_b}{k}.$$

Hence, in S_b contention happens only in the multiplexing stage and this contention has the same characteristics of contention at AWG stage in S_a. Therefore,

$$\pi_a = \pi_b.$$

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Optical transport
network

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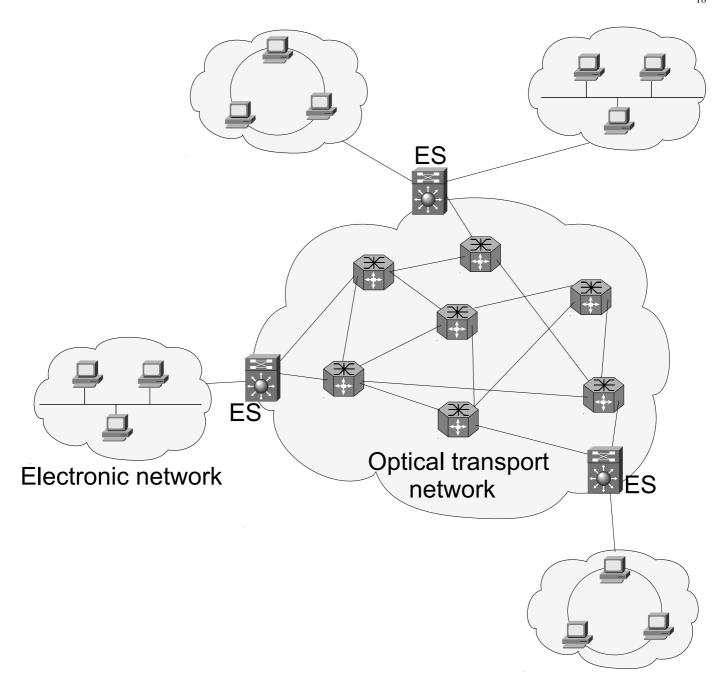
Electronic network

ES

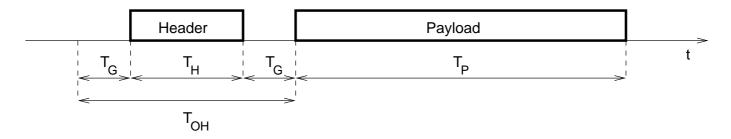Fig. 1.   The optical transport network architecture

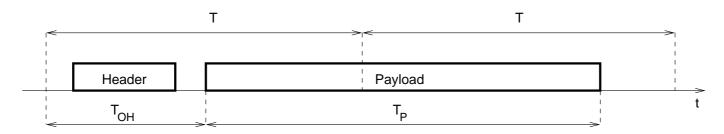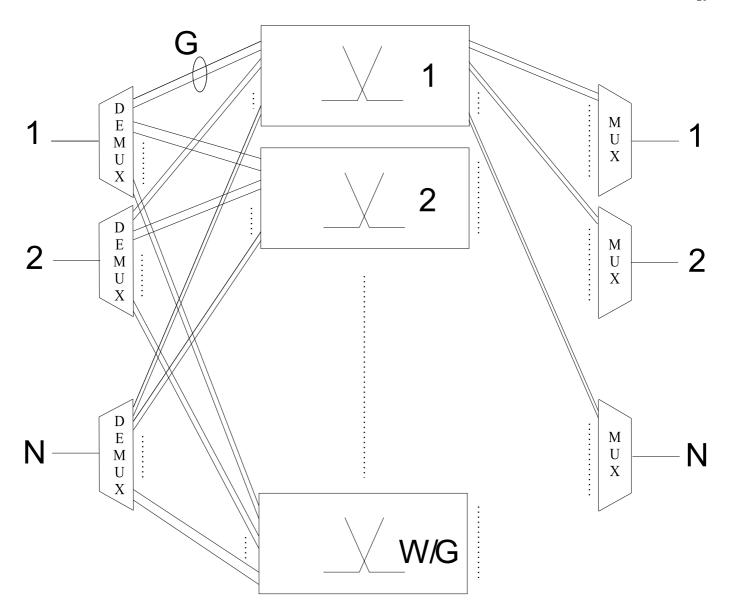Fig. 2.   Optical packet format.

Fig. 3.   Optical packet and time-slots.

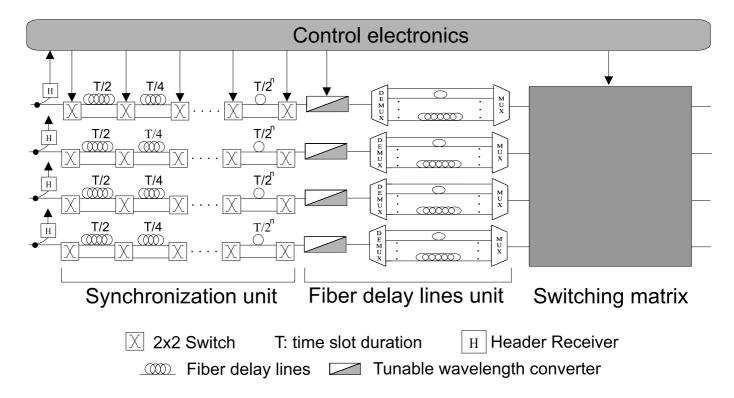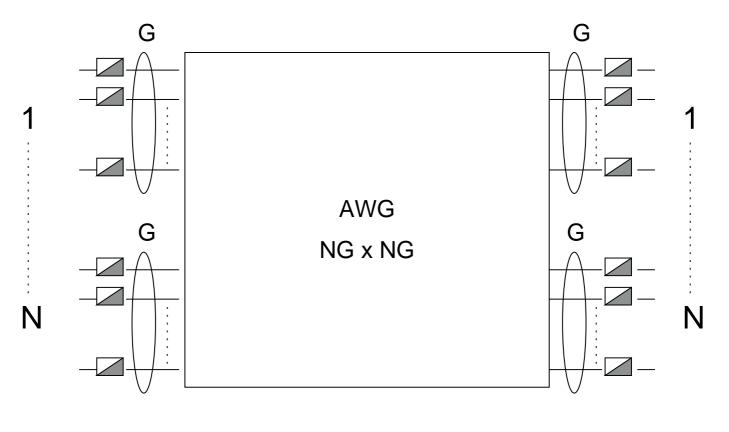Fig. 4.   Optical packet-switching node general architecture

Fig. 5. Detailed structure of one of the W/G parallel switching planes

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TWC: Tunable Wavelength Converter

Fig. 6.   Switching matrix with structure (a)

$$\lambda_1^1 \quad \lambda_2^1 \quad \lambda_3^1 \quad \lambda_4^1$$

$$\lambda_1^2 \quad \lambda_2^2 \quad \lambda_3^2 \quad \lambda_4^2$$

$$\lambda_1^3 \quad \lambda_2^3 \quad \lambda_3^3 \quad \lambda_4^3$$

$$\lambda_1^4 \quad \lambda_2^4 \quad \lambda_3^4 \quad \lambda_4^4$$

AWG

$$\lambda_1^1 \quad \lambda_2^2 \quad \lambda_3^3 \quad \lambda_4^4$$

$$\lambda_4^1 \quad \lambda_1^2 \quad \lambda_2^3 \quad \lambda_3^4$$

$$\lambda_3^1 \quad \lambda_4^2 \quad \lambda_1^4 \quad \lambda_2^4$$

$$\lambda_2^1 \quad \lambda_3^2 \quad \lambda_4^3 \quad \lambda_1^4$$

Fig. 7.   AWG routing scheme

Fig. 8.   Switching matrix with structure (b)

Fig. 9.   Switching matrix with structure (c)
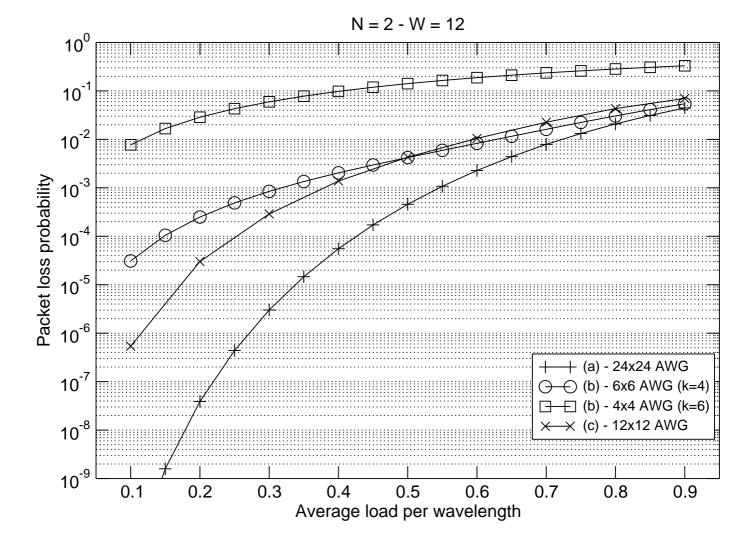
Fig. 10. Multi-plane node using structure (c).

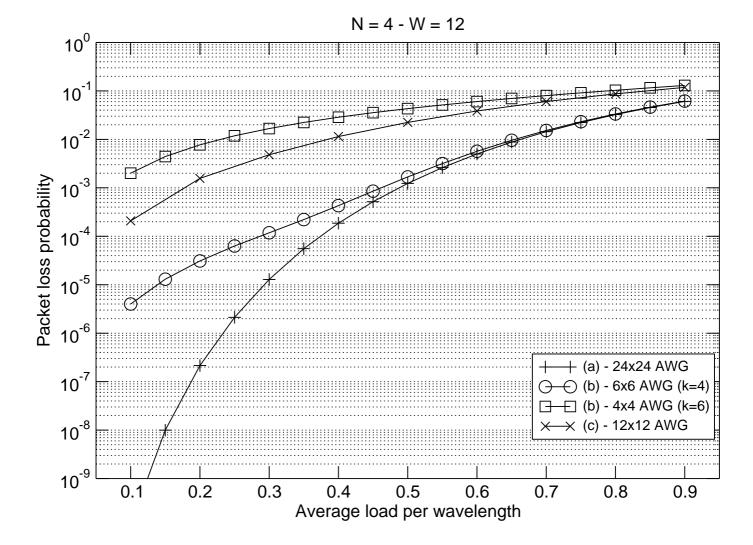Fig. 11. Packet loss probability of different structures, with $N = 2$, $W = 12$.

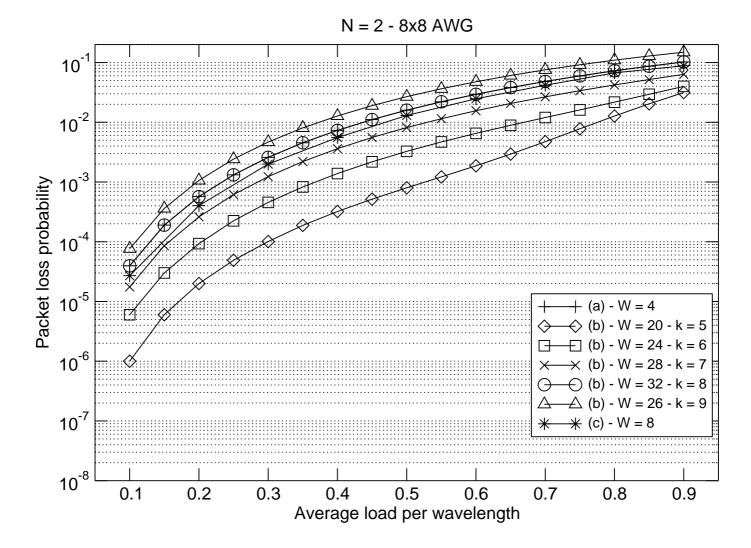Fig. 12.   Packet loss probability of different structures, with $N = 4$, $W = 12$.

Fig. 13.   Packet loss probability of different 8×8 AWGs.

	(a)	(b)	(c)
AWG size	$NW \times NW$	$NW/k \times NW/k$	$W \times W$
TWC	$2NW$	$NW + (NW/k)^2$	NW
MUX / DEMUX size	- / -	$k \times 1$ / $1 \times k$	$N \times 1$ / -
MUX / DEMUX count	- / -	NW/k / NW/k	W / -

TABLE I

COMPONENTS OF THE THREE STRUCTURES, KEEPING N AND W CONSTANT.

	(a)	(b) - $k = N$	(c)
AWG count	N	1	1
TWC	$2NW$	$NW + W^2$	NW
MUX / DEMUX size	-	$N \times 1$ / $1 \times N$	$N \times 1$/ -
MUX / DEMUX count	-	W / W	W / -

TABLE II

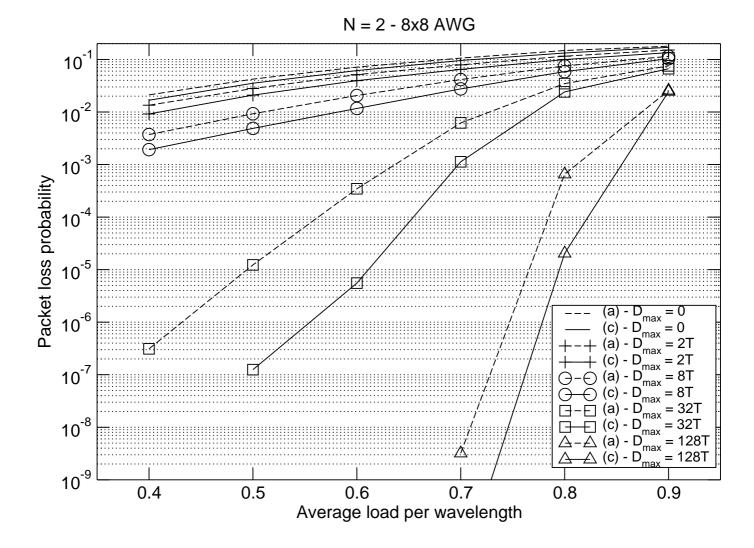COMPONENTS OF THE THREE STRUCTURES, KEEPING AWG SIZE CONSTANT.

Fig. 14.   Packet loss probability of structures (a) and (c) with $N = 2$ and 8×8 AWGs, for different values of D_{max}.
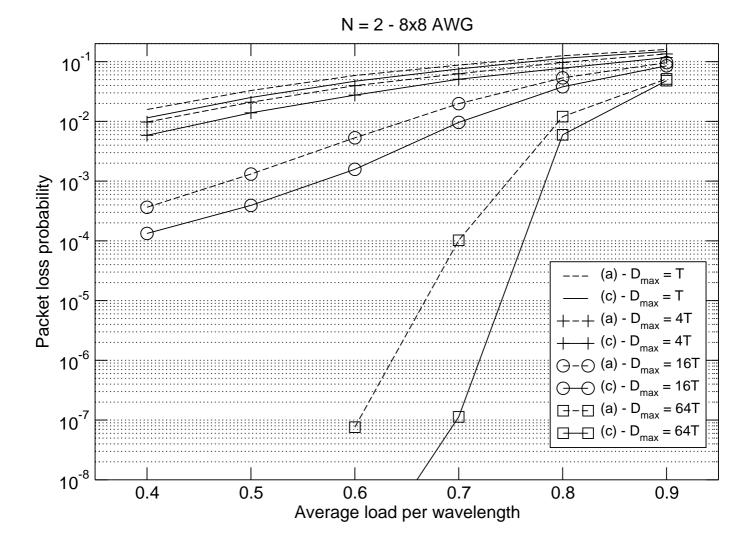
Fig. 15. Packet loss probability of structures (a) and (c) with $N = 2$ and 8×8 AWGs, for different values of D_{max}.
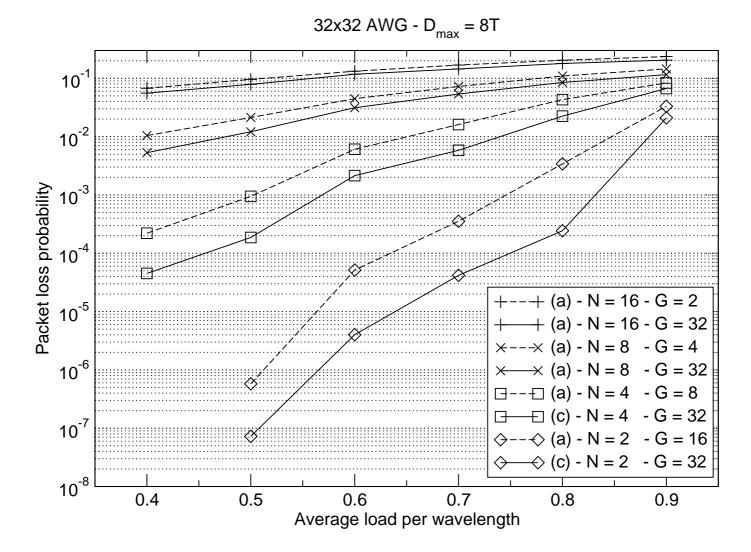
Fig. 16. Packet loss probability of structures (a) and (c) with 32×32 AWGs, for different values of G.